PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Garlapati et al.

Title: VOLTAGE REFERENCE GENERATOR CIRCUIT USING LOW-BETA EFFECT OF A CMOS BIPOLAR TRANSISTOR

Application No.: 10/813,837 Filed: March 31, 2004

Examiner: Not yet assigned Group Art Unit: 2819

Atty. Docket No.: 026-0044

July 14, 2004

Mail Stop Amendment
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☒ Form(s) PTO-1449 (2 pages), including copy(ies) of 9 reference(s).
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to the Examiner's attention in the above-identified application. Citation of such information shall not be construed as:

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For each item of information listed that is not in the English language, the undersigned has provided a concise explanation of the relevance through (i) an English language abstract, (ii) an English language equivalent application, or (iii) if cited in a search report or other action

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☐ This Information Disclosure Statement is filed within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d) or within three months of entry of the national stage as set forth in § 1.491 in an international application. Therefore, no fee is required.

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Nicole Teitler Cave 7/14/04
Nicole Teitler Cave Date

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Respectfully submitted,

Nicole Teitler Cave, Reg. No. 54,021
Attorney for Applicant(s)
(512) 338-6315
(512) 338-6301 (fax)

U.S. Department of Commerce, Patent and Trademark Office	**Attorney Docket No.:** *026-0044*
	Application No.: *10/813,837*
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	**Applicant(s):** *Garlapati et al.*
(Use several sheets if necessary)	**Filing Date:** *March 31, 2004*
	Group Art Unit: *2819*
	Date Submitted: *July 14, 2004*

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name
	AA	4,588,941	May 13, 1986	Kerth et al.
	AB	4,857,823	Aug. 15, 1989	Bitting
	AC	5,001,362	Mar. 19, 1991	Tran
	AD	5,132,556	Jul. 21, 1992	Cheng
	AE	5,488,329	Jan. 30, 1996	Ridgers
	AF	5,568,045	Oct. 22, 1996	Koazechi
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	AI	5,796,244	Aug. 18, 1998	Chen et al.
	AJ	5,900,773	May 4, 1999	Susak
	AK	6,031,365	Feb. 29, 2000	Sharpe-Geisler

Foreign Patent Documents

					Translation	
		Document	Date	Country	Yes	No
	AL	JP 1292411 (English abstract)	Nov. 24, 1989	Japan		

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AM	Allen et al., "Current and Voltage References," CMOS Analog Circuit Design, 1987, pp. 240-252.
	AN	Allen et al., "CMOS Analog Circuits and Systems," CMOS Analog Circuit Design, 1987, pp. 589-599.
	AO	Banba et al., "A CMOS Bandgap Reference Circuit with Sub-1-V Operation," IEEE Journal of Solid-State Circuits, Vol. 34, No. 5, May, 1999, pp. 670-674.

Examiner	**Date Considered**

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name
	AP	6,052,020	Apr. 18, 2000	Doyle
	AQ	6,075,407	Jun. 13, 2000	Doyle
	AR	6,160,391	Dec. 12, 2000	Banba
	AS	6,366,071	Apr. 2, 2002	Yu

Foreign Patent Documents

					Translation	
		Document	Date	Country	Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AT	de Langen et al., "Compact Low-voltage PTAT-Current Source and Bandgap-Reference Circuits," Delft Institute for MicroElectronics and Submicron technology (DIMES), pp. 108-111.
	AU	Gray et al., "Band-Gap-Referenced Biasing Circuits," Analysis and Design of Analog Integrated Circuits, Third Edition, 1993, pp. 338-346.
	AV	Lee, "Bandgap References in CMOS Technology," The Design of CMOS Radio-Frequency Integrated Circuits, 1998, pp. 233-235.
	AW	Razavi, "Bandgap Reference," Design of Analog CMOS Integrated Circuits, 2001, pp. 384-392.
	AX	Phang et al., "Low Voltage, Low Power CMOS Bandgap References," ECE 1352, University of Toronto, pp. 1-17.

Examiner	**Date Considered**

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